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NEW SCHEME

Third Semester B.E Degree Examination, July 2006
CS / IS / EC / TE / EE / IT / ML / BM
Logic Design

Time: 3 hrs.] [Max. Marks: 100

Note: *1. Answer any FIVE full questions.*

1 a. State and explain with examples shannon's expansion and reduction theorems in Boolean algebra. **(04 Marks)**

b. Simplify the following using Boolean theorems:

i) $f(x, y, z) = (x+y)[\overline{x}(\overline{y}+\overline{z})] + \overline{x}\overline{y} + \overline{x}\overline{z}$

ii) $f(A, B, C) = (A+B+C)(\overline{A}+B+C)(\overline{A}+B+\overline{C})$ **(08 Marks)**

c. Transform each of the following canonical expressions into other canonical form in decimal notation and express in simplified form in decimal notation and express in simplified form

i) $f(x, y, z) = \sum m(0, 1, 3, 4, 6, 7)$

ii) $f(w, x, y, z) = \prod m(0, 1, 2, 3, 4, 6, 12)$ **(08 Marks)**

2 a. What are don't care condition? What are its advantages? **(04 Marks)**

b. Obtain a NOR-gate realization of the Boolean expression, $f(w, x, y, z) = \sum m(0, 3, 5, 6, 9, 10, 12, 15)$ **(08 Marks)**

c. Obtain a NAND-gate realization of the Boolean expression $f(A, B, C) = (A+\overline{B}+C)(\overline{A}+\overline{B}+\overline{C})(\overline{A}+B)$ **(08 Marks)**

3 a. Determine the minimal sum-of-product (SOP) expression for $f(w, x, y, z) = \sum(0, 2, 4, 9, 12, 15) + \sum d(1, 5, 7, 10)$ **(08 Marks)**

b. Using Quine-Mcluskey method and prime implicant reduction, determine the minimal product-of-sums (POS) expression for the following using decimal notation $f(w, x, y, z) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + \sum d(4, 8, 11)$ **(08 Marks)**

c. Reduce the given switching function using single variable map technique $f(A, B, C, D) = \sum m(0, 1, 4, 7, 10, 14)$ **(04 Marks)**

4 a. Define the following terms:

i) Fan-in and Fan-out ii) The propagation delay **(06 Marks)**

b. What is the principle of operation of an schottky TTL? Explain with a circuit diagram the operation of a schottky TTL **(08 Marks)**

c. A TTL gate is generated to sink 10mA without exceeding an output voltage VOL=0.4V and to source 5mA without dropping below VOH = 2.4V. If I_{IH} =100mA at 2.4V and I_{IH} = 1mA at 0.4V, calculate the 0-state and 1-state fan-outs. **(06 Marks)**

5 a. With a block diagram describe the principle of operation of a carry Look-ahead-adder. **(06 Marks)**

b. What is a Programmable LOGIC Array (PLA)? Describe with a logic diagram the principle of operation of a PLA. What are its advantages? **(08 Marks)**

c. Implement the following Boolean function using 8:1 multiplexer. $F(A, B, C, D) = \overline{A}B\overline{D} + ACD + \overline{B}CD + \overline{A}\overline{C}D$. **(06 Marks)**

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6 a. What is a sequential circuit? Discuss the different types of sequential circuits. **(06 Marks)**

b. With a neat logic diagram and timing waveforms describe the operation of a master-slave JK flip-flop. **(06 Marks)**

c. A stable assignment table for a mod-5 counter is given below:

S	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	1
3	1	1	1
4	1	1	0

Derive a counter configuration. **(08 Marks)**

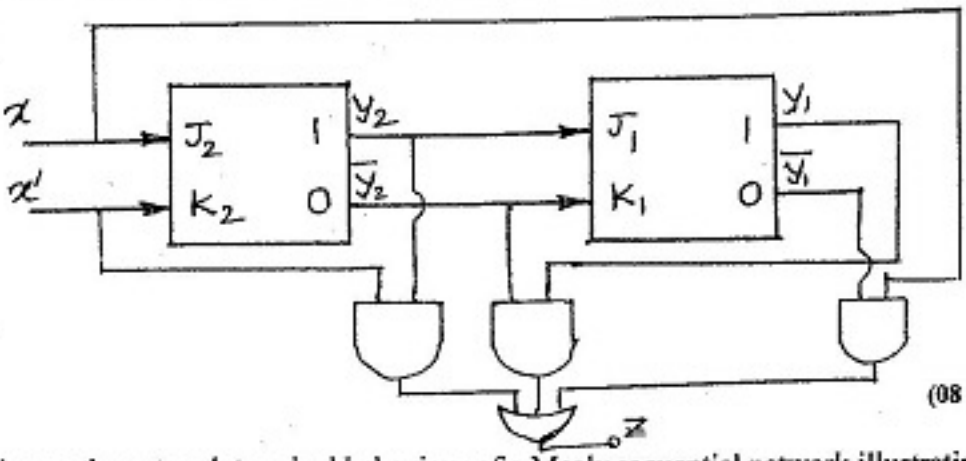
7 a. Explain with sketches the Mealy model and the Moore model sequential networks. **(06 Marks)**

b. Analyze the synchronous circuit of the Fig. (clock not shown but is implicit)

i) Write down the excitation and output functions

ii) Form the excitation and state tables

iii) Give a word description of the circuit operatin.



(08 Marks)

c. Discuss the network terminal behaviour of a Mealy sequential network illustrating the occurrence of false output with timing diagrams. **(06 Marks)**

8 Write short notes on:

i) Principle of duality

ii) Compansion of logic families

iii) CMOS inverter

iv) Programmable Read-only memories. **(20 Marks)**

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